TECHNICAL REPORT 2052
September 2014

Time-Domain Switched Accelerometer Design and Fabrication

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ADMINISTRATIVE INFORMATION

The work described in this report was performed by the Advanced Integrated Circuit Technology Branch (Code 55250) of the Communications Division (Code 55200), Space and Naval Warfare Systems Center Pacific (SSC Pacific), San Diego, CA. The Naval Innovative Science and Engineering (NISE) Program at SSC Pacific funded this Applied Research project.

Released by
B. Offord, Acting Head
Advanced Integrated Circuit
Technology Branch

Under authority of
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Communications Division

SB

EXECUTIVE SUMMARY

OBJECTIVE

The objective of this report is to record the decision-making process for developing the device design and fabrication workflow for the time-domain switched accelerometers (TDSA) developed as part of the Naval Innovative Science and Engineering (NISE)-funded project "Time Domain Switching Proof Mass Proximity Switch Utilization for Inertial Navigation."

METHOD

The design and fabrication of these devices was based on using a sacrificial layer that both defines a capacitive gap for a sliding, non-contact proximity switch and frees a wafer-thick proof-mass to vibrate in the plane of the wafer.

CONCLUSION AND RECOMMENDATIONS

Time-domain switched accelerometers can be built using a three-mask process. The vacuum-sealing process described in this report is conducted at a low temperature and can be used to vacuum pack the devices on wafer,

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INTRODUCTION

Time-domain switched inertial sensors (TDSIS) consist of a driven mass-on-a-spring harmonic oscillator and at least two proximity switches that provide a digital trigger when the oscillating mass passes two different known locations (see Figure 1) [1]. Inertial forces are determined by fitting the measured time intervals between triggering events to the equations of motion for a harmonic oscillation displaced by an inertial force [1, 2]. This report describes the design considerations and device fabrication challenges of a time-domain switched accelerometer (TDSA).

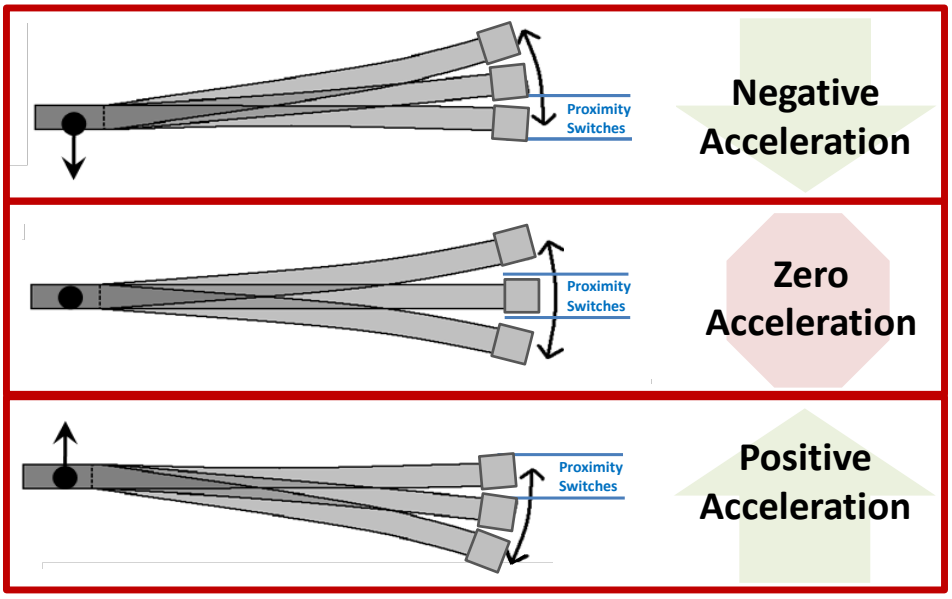


Figure 1. General operation of a time domain switched accelerometer.

DESIGN CONSIDERATIONS

Although TDSIS's are not limited to micro-electro-mechanical systems (MEMS), a MEMS-based device is highly desirable because of its small size and reduced fabrication cost. To take advantage of well-established silicon processing techniques, the spring and proof-mass were chosen for fabrication out of a highly doped n-type (conductive) silicon wafer. Having the conductive proof-mass pass near a biased electrode provides a current pulse. Depending on the amount of current involved, this current pulse can directly trigger a digital input, or be amplified and then trigger a digital input. Since the switch electrode does not make physical contact with the proof-mass, it does not interfere with the proof-mass's harmonic oscillation. A well-defined passing distance on the order of tens of nanometers optimizes the switch performance. In semiconductor processing, such dimensions are more easily defined in the vertical direction by thin layer growth than across the plane of the wafer, using lithography and thin film patterning. Therefore, a design was chosen with an asymmetric spring that allows motion within the plane of the wafer, but inhibits motion in the vertical direction. This is accomplished by making the thickness of the spring (vertical direction) 10 times greater than the width of the spring (horizontal direction). A cantilevered proof-mass on a spring was chosen to minimize device size for a given harmonic oscillation amplitude.

Figure 2 shows the general concept of the sliding proof-mass proximity switches. However, putting the fixed electrodes of the proximity switches on either side of the proof-mass limit the

ability to use capacitive forcing to drive the harmonic oscillation. Therefore, the proximity switch fixed electrodes were placed inside the proof-mass so that the full cross section of the proof-mass could be used as a parallel plate capacitor to capacitively drive the harmonic oscillator (Figure 3). In this design, two springs are used instead of one to increase the capacitive driving force oscillating the proof-mass.

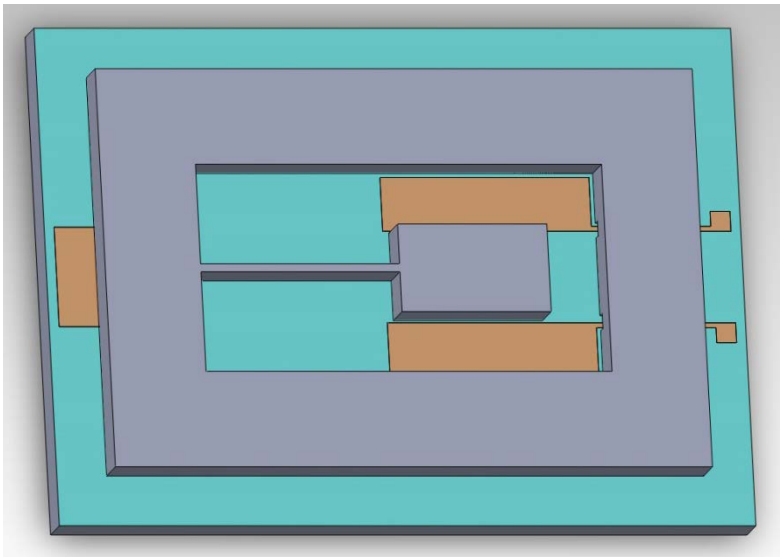


Figure 2. Sliding proximity switches using a vertically defined gap.

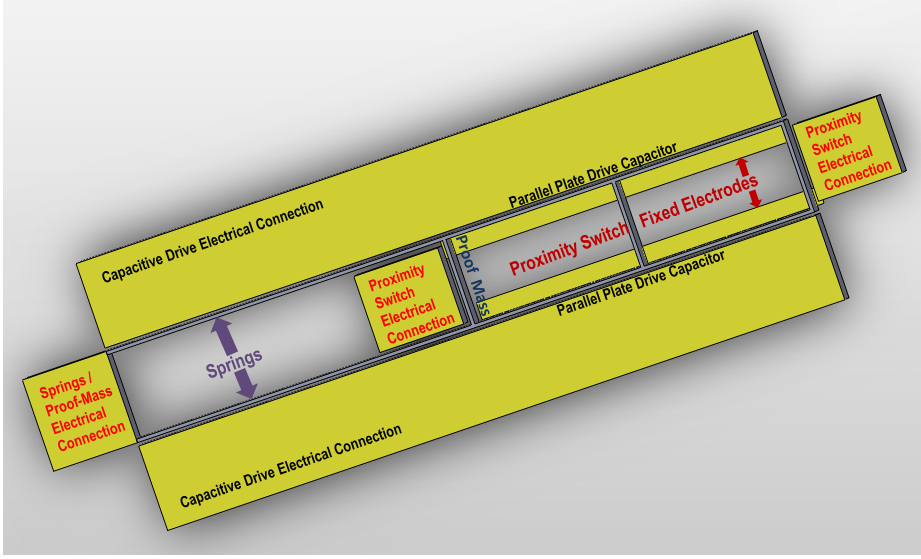


Figure 3. Internal proximity switch electrodes, external driving electrodes.

The design shown in Figure 4 increases the proximity switch current by increasing the area between the proof-mass and fixed electrode.

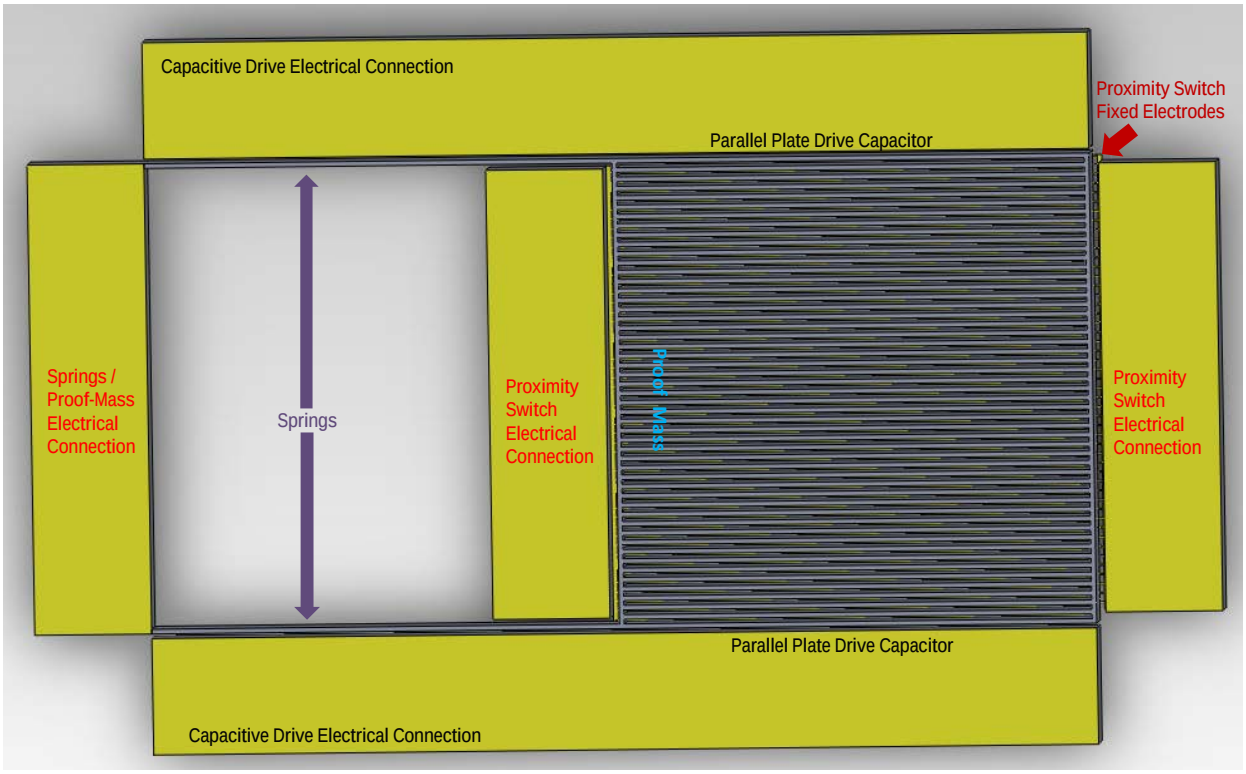


Figure 4. Proximity switches with larger over-lap area.

DEVICE REQUIREMENTS

The principle requirements for the device described are:

- The mass on a spring harmonically oscillates in only one direction
- Capacitive force used to drive oscillation
- Conductive proof mass
- Proof-mass passes fixed conductive electrodes during oscillation
- Proximity switch does not interfere with harmonic oscillation and produces a digital trigger with minimum timing jitter

The Spring

The spring(s) consist of 40-µm by 400-µm by 4-mm long silicon bars formed by deep silicon (Si) etching through a 400-µm-thick silicon wafer. The asymmetric cross section of the spring is to promote bending within the plane of the wafer while inhibiting bending in the vertical direction. This is necessary since the spring and the proof mass are suspended above the supporting base by a thin gap defined by the thickness of a sacrificial silicon dioxide layer, which is removed after the proof mass/spring wafer is bonded to the base wafer, then the deep etch defining the spring(s) and the proof-mass is performed. One side of the spring connects to the free-floating proof-mass while the

other side is connected to a section of the proof-mass spring wafer, which remains bonded to the base wafer.

The Proof-Mass

To easily etch the sacrificial oxide under the proof-mass (and springs), no part of the proof-mass (and springs) is greater than 40-µm wide. Therefore, the proof-mass consists of a grating structure made of 40-µm by 400-µm cross-section beams. Because these beams are identical in cross section to the springs, it is important that any vibrational resonance of these beams have an oscillation frequency much greater than the spring—proof-mass structure as a whole.

The Supporting Base

The silicon deep etch etches through the proof-mass wafer, creating electrically isolated islands of silicon. To maintain structural integrity, before the deep etch begins, the proof-mass wafer is bonded to a bare silicon wafer using a low vapor pressure epoxy. This creates a topologically independent bond that does not require alignment. Before the epoxy is cured, the bonded wafers are pressed to ensure the final device thickness is within dicing limits. Adhesive bonding was chosen over eutectic bonding to make the fabrication process easier and more robust.

The removal of the sacrificial oxide layer frees the spring and proof-mass from the base wafer to allow harmonic oscillation while leaving the fixed electrodes attached to the base wafer. The fixed electrodes are also ohmicly contacted to electrically isolated conductive silicon pillars, which will be flip-chip bonded to wire traces on transparent quartz substrate. The quartz substrate will provide electrical contacts to supporting test circuitry, as well as an optical window to observe device operation.

The Proximity Switches

The proximity switch described can produce a current pulse by two different mechanisms: (1) electron tunneling across the gap between the fixed electrode and the moving proof-mass, and (2) capacitive charge build-up when the area of the proof-mass passes over the area of the fixed electrode. Electron tunneling produces a pulse of current when the electric field between the fixed electrode and the proof-mass is at its peak, when the two edges are at their closest distance. The current caused by the sudden change of capacitance is proportional to how quickly the fixed electrode/proof-mass overlap area changes. (The devices optimize the capacitive current by optimizing the overlap between the fixed electrodes and the proof-mass and minimizing the gap formed by removing the sacrificial oxide layer.) The amount of current generated by the capacitive switch increases as the velocity of the proof-mass increases, and thus increases with the operating harmonic frequency of the spring-proof-mass system. Unlike the tunneling current, the capacitive current can directly switch a logic circuit without signal amplification. This is important since signal amplification itself can produce timing jitter, which is the main cause of error in TDSIS.

The Oscillation Frequency

The springs and proof-masses were chosen to produce a resonant frequency in the range of 1 to 10 kHz. The higher the operating frequency, the greater the frequency response of the device, and the smaller the physical displacement associated with an external force or the driving force. In addition, the higher the operating frequency, the shorter the time intervals measured, and thus the smaller the measurement resolution. Because the device design uses parallel plate capacitive forcing to drive the proof-mass oscillation, the effective spring constant, and thus the resonant frequency, can be adjusted

by applying a DC offset to the drive capacitors. This can be used to optimize the accelerometer's dynamic range, as well as the capacitive proximity switch performance.

FABRICATION CONSIDERATIONS

FABRICATION REQUIREMENTS

The device fabrication must provide the following:

- Define deep etch pattern for proof-mass definition, spring definition, and electrical isolation
- Define sacrificial layer that separates the proof-mass from the fixed electrodes (and frees the springs and proof-mass from the base
- Define fixed electrode traces
- Ensure that each pattern definition (and sacrificial layer etch) does not damage the other structures
- The wafer that is deep silicon etched through the entire wafer must be secured to a unprocessed base wafer before the deep etch.

Patterned Features

Three structures require pattern definition by photolithography:

- The through wafer deep silicon etch that defines the proof-mass, springs, and provides electrical isolation between the proof-mass and the fixed electrodes
- The sacrificial layer that defines which structures are free-floating and which structures are physically connected to the base wafer
- The fixed electrodes that act as digital proximity switches

The through-wafer deep silicon etch is performed by an Oxford Plasmalab® 100RIE/ICP using SF_6 /C_4F_8 plasma. The best etch mask for the deep silicon etch is several hundred nanometers of chromium. The same surface needed to be masked for the deep silicon etch also needs a metallization compatible with flip-chip ball bonding. Unfortunately, chromium is not such a metallization. The solution is to have final metallization (Cr – Au) under the etch mask (Cr) with a titanium sacrificial layer between the two to expose the gold surface before flip-chip bonding. A lift-off mask consisting of an aluminum layer thicker than the Cr-Au-Ti-Cr stack would define the entire Cr-Au-Ti-Cr stack, and a photo resist patterned in the reverse image of the Cr-Au-Ti-Cr Deep etch mask pattern. Masked by the patterned photo resist, the aluminum would be slightly over-etched, creating an over-hang of photo resist on the edges of the Cr-Au-Ti-Cr lift-off mask. After the Cr-Au-Ti-Cr is deposited, the photo resist and aluminum would be removed using acetone and aluminum etch consecutively.

On the opposite side of the wafer, a silicon dioxide sacrificial layer is deposited using plasma enhanced chemical vapor deposition (PECVD) at a thickness that defines the gap between the proof-mass and the fixed electrodes. This silicon dioxide layer is patterned with an etch masked with patterned photo resist aligned to the Cr-Au-Ti-Cr patterned metallization. The fixed electrodes consist of a Cr-Au-Cr layer patterned over the sacrificial silicon dioxide (SiO_2) layer, using an aluminum–photo resist lift-off. The aluminum layer is left in place to be removed by the same etch as the sacrificial oxide. A 300-nm layer of PECVD silicon nitride is used as a blanket cover over the sacrificial SiO_2, the Cr-Au-Cr fixed electrodes, and the temporary aluminum layer, to protect the

wafer bonding from the hydrogen fluoride (HF) etch that removes the sacrificial SiO_2 and aluminum. (The aluminum protects the silicon nitride from the deep silicon etch, and is removed when the sacrificial oxide is removed with a HF etch.)

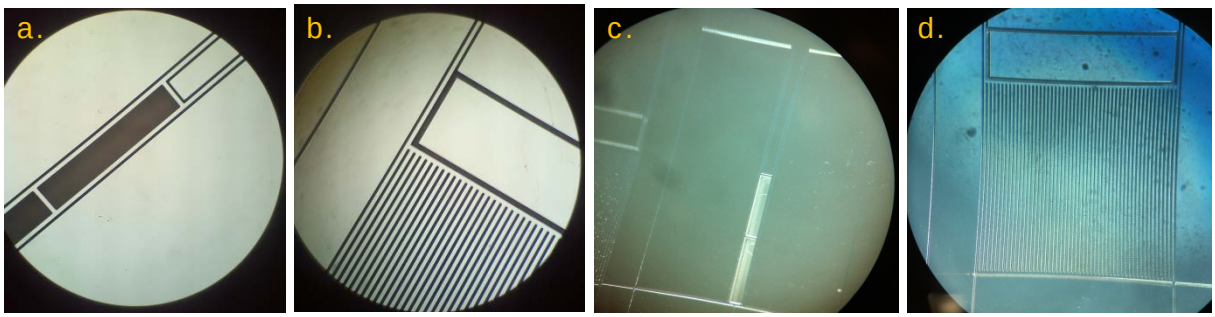


Figure 5. a. Metallization/deep Si etch mask for two fixed electrode design, b. metallization/deep Si etch mask for 100 fixed electrode design, c. deep etched two fixed electrode design, d. deep etched 100 fixed electrode design.

Critical Alignments

It is critical that the front metallization and back metallization are as well-aligned as possible since this alignment defines the locations when the proximity switches produce their digital trigger. The front to back alignment accuracy of the Karl Suss® MA6 Mask Aligner is 1 µm. To make up for this possible error, a calibration test with a known external force (gravity) is used to accurately determine the trigger positions. The alignment of the sacrificial oxide layer patterning to the deep etch pattern is less critical since a 5-µm overlap is built into the design.

Wafer Bonding

The proof-mass wafer is bonded to a blank silicon wafer to support the structures separated by the silicon deep etch. A low vapor pressure epoxy (Torr Seal®) is used to create a conformal seal across the silicon nitride layer covering the patterned fixed electrodes and the patterned sacrificial oxide and aluminum layers. A fixed weight of epoxy and a consistent pressing force is used to create a consistent bond.

Etch Selectivity

Three etches are used during the fabrication process: (1) the SF_6 dry etch is used to pattern the sacrificial silicon dioxide layer, (2) the SF6/C_4F_8 deep silicon etch that defines and electrically isolating the proof-mass and springs, and (3) the HF etch used to remove the sacrificial silicon oxide and aluminum that free the proof-mass and springs. The silicon nitride layer protects the epoxy from the HF etch. The aluminum is designed to protect the silicon nitride from the deep silicon etch and decrease the time required to etch the sacrificial silicon dioxide layer. The top chromium layer of the Cr-Au-Ti-Cr metallization is used as the etch mask for the deep silicon etch. The Ti layer etches in the HF etch to remove the chromium (Cr) etch mask so that the gold ball bonds used for flip-chip bonding will adhere to the metallization. The HF etch must not blister or peal the metallizations on either side of the proof-mass wafer. Thermally evaporated metallization holds up better than sputtered metallizations. In addition, using a vapor HF etching system instead of a wet HF etch would prevent damage to the metallizations and eliminate the need for stiction, eliminating critical point drying after the HF etch.

Surviving Dicing

A dicing saw separates the individual devices. During dicing, the wafer is sprayed with high-pressure water that can damage the proof-mass and springs. Therefore, the proof-mass and springs are not freed by the HF etch until after dicing.

Removing Sacrificial Layer

The sacrificial silicon dioxide layer is removed by either using a wet HF etch on the individual diced die, followed by rinsing and critical point drying, or by HF vapor etching the individual die.

DEVICE PACKAGING

PACKAGING REQUIREMENTS

The device packaging must provide the following:

- Provide electrical connections
- Vacuum seal spring / proof-mass structure
- Provide window to observe proof-mass motion

Flip-Chip Bonding

After dicing and proof-mass release, the device needs to be electrically contacted and vacuum sealed on five sides. What is now the top side needs to be sealed with an off-set to allow the proof-mass to move without contacting the packaging. Flip-chip ball bonding provides electrical contact to wire traces on a larger substrate and provides the off-set required for harmonic oscillation. The four remaining edges can be sealed with a low out-gas epoxy such as Torr Seal®.

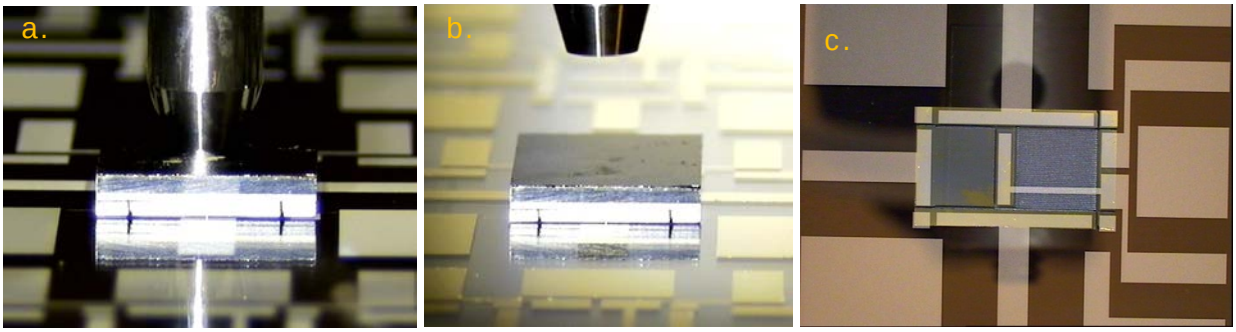


Figure 6. a. and b. Die flip-chip bonded to wire traces on a quartz substrate, c. flip-chip boded device as seen from the opposite side of the transparent quartz substrate.

Vacuum Sealing

Three of the four remaining edges are sealed with Torr Seal® under atmospheric conditions. After the Torr Seal® has cured, fresh Torr Seal® is applied to the final edge and placed vertically in a vacuum chamber with the unsealed Torr Seal® up. As the vacuum chamber is pumped down, the gas in the proof-mass chamber bubbles up through the uncured epoxy, with the Torr Seal® resealing the chamber after the gas has escaped. The packaged device is left in the vacuum chamber until the epoxy has cured.

Shielding Noise

The wire traces on the substrate connect the flip-chip ball bonds to board-edge SMA connectors, providing coaxial shielding to the time interval trigger located at the output port. The coaxial cables to a time interval analyzer will eliminate switching time jitter caused by electronic noise.

CONCLUSION

Time-domain switched accelerometers were designed for performance and ease of manufacturing. A fabrication workflow was established (see Appendix A). Fabrication and performance issues were identified and addressed.

REFERENCES

1. P. D. Swanson, C. H. Tally, and R. L. Waters. 2011. "Proposed Digital, Auto Ranging, Self Calibrating Inertial Sensor," *2011 IEEE Sensors* (pp. 1457–1460). Oct. 28-31. Limerick, Ireland. IEEE.

2. C. H. Tally, P. D. Swanson, and R. L. Waters. 2012. "Intelligent Polynomial Curve Fitting got Time-Domain Triggered Inertial Devices." *Proceedings of the 2012 IEEE/ION Position, Location and Navigation Symposium* (pp. 1–7). April 23–26, Myrtle Beach, SC. IEEE.

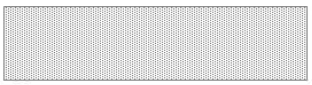
APENDIX A: THREE-MASK PROCESS FLOW - TIME DOMAIN SWITCHING

Process Flow — Back-side Contact Layer / Deep Etch Mask — Steps 1-13

Step	Layer	Code	Process Side	Description
1		WSTR		Wafer Start (DSP Si 400um)
2			Back	Deposit 600nm of Aluminum
3	CNT	COAT	Back	Coat "V3-3 SSCPAC CAP ACCEL GYRO: 1 Back Deep Si Etch Pattern"
4	CNT	XPOS	Back	Align/Expose "1 Back Deep Si Etch Pattern"
5	CNT	PDEV	Back	Develop "1 Back Deep Si Etch Pattern"
6			Back	Etch Al to create photo resist over-hang
7			Back	Evaporate 40nm Cr
8			Back	Evaporate 320nm Au
9			Back	Evaporate 100nm Ti
10			Back	Evaporate 100nm Cr
11			Back	Lift-off metal layers with Acetone or PR Stripper
12			Back	Remove Aluminum in Aluminum etch
13			Back	O2 plasma Descum

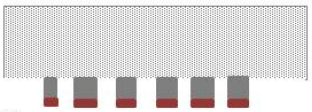
Process Flow Cross-Sections

Step 1

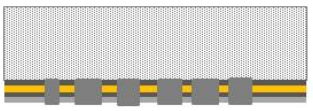


Step 2

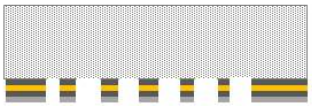
Step 5



Step 11



Step 12



Reticle Info

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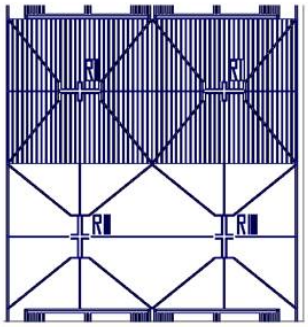
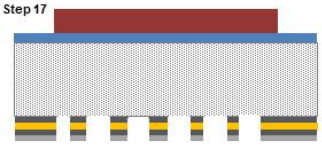


Process Flow — Front-side Sacrificial Oxide Layer — Steps 14-19

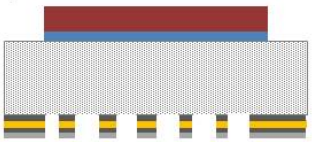
Step	Layer	Code	Process Side	Description
14	SAC	SIO	Front	PECVD Silicon Dioxide 100nm
15	SAC	COAT	Front	Coat "Sacrificial Oxide layer"
16	SAC	XPOS	Front	Align/Expose "Sacrificial Oxide Layer"
17	SAC	PDEV	Front	Develop "Sacrificial Oxide Layer"
18	SAC	POXE	Front	Dry Etch Silicon Dioxide 500nm (Stop on Silicon)
19	SAC	ASHR	ASHR	Ash/ Strip Resist

Process Flow Cross-Sections

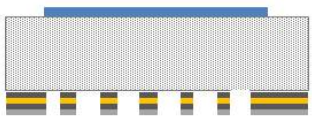
Step 17



Step 18



Step 19



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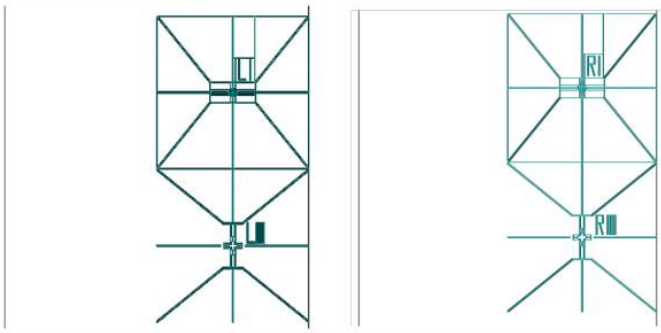
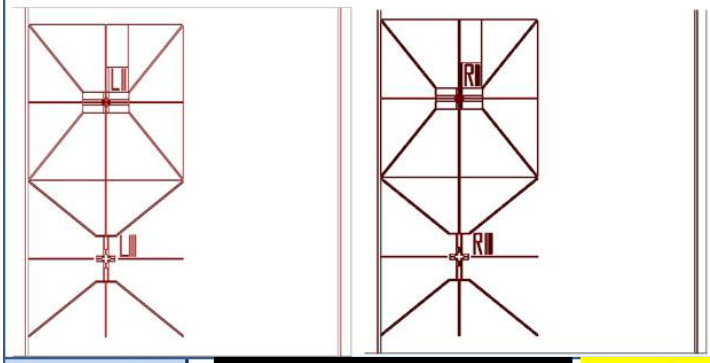


Process Flow — Front-side Metal Layer — Steps 20-30

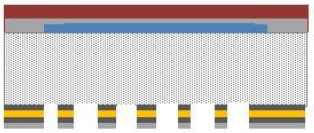
Step	Layer	Code	Process Side	Description
20			Front	Deposit 450nm of Aluminum
21	CNT	COAT	Front	Coat "V3-3 SSCPAC CAP ACCEL GYRO: 3 Front Metal"
22	CNT	XPOS	Front	Align/Expose "3 Front Metal"
23	CNT	PDEV	Front	Develop "3 Front Metal"
24			Front	Etch Al to create photo resist over-hang
25			Front	Evaporate 40nm Cr
26			Front	Evaporate 100nm Au
27			Front	Evaporate 40nm Cr
28			Front	Lift-off metal layers with Acetone or PR Stripper
29			Front	O2 plasma Descum
30	SAC	SIO	Front	PECVD Silicon Nitride 200nm

Reticle Info

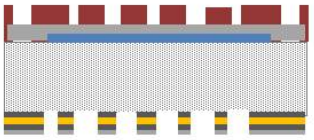


Process Flow Cross-Sections

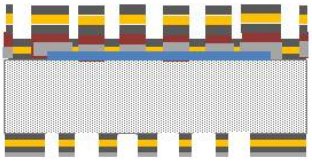
Step 21



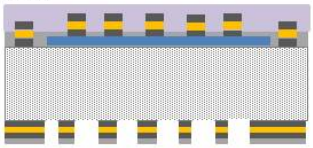
Step 23



Step 27



Step 30

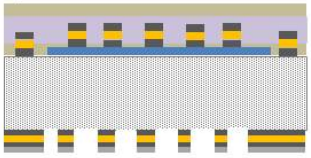


Process Flow — SU8 Layer and Wafer Bonding — Steps 31-33

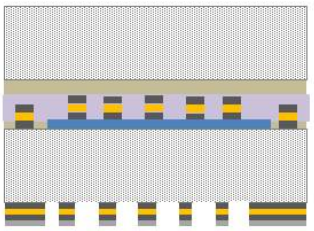
Step	Layer	Code	Process Side	Description
31	BOND	TORR	Front	Coat TorrSeal
32	BOND	WAFR	Front	Bond intrinsic Si Wafer
33	BOND	CURE	Front	Cure TorrSeal

Process Flow Cross-Sections

Step 21



Step 32

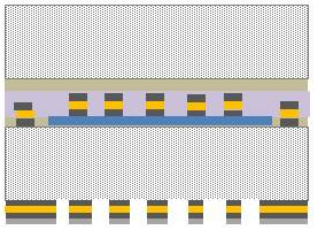


Process Flow | Back Deep Si | Step 34

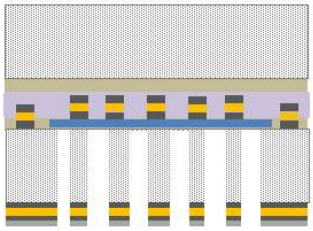
Step	Layer	Code	Process Side	Description
34	DEEP	POXE	Back	Deep Reactive Ion Etch Si 400µm

Process Flow Cross-Sections

Step 34



Step 34

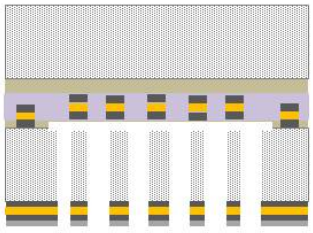


Process Flow | Release | Steps 35-36

Step	Layer	Code	Process Side	Description
35				Dice Wafer
36	DEEP	RELS	Back	HF Critical Pt Dry Release

Process Flow Cross-Sections

Step 36



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14. ABSTRACT

The objective of this report is to record the decision-making process for developing the device design and fabrication workflow for the time-domain switched accelerometers (TDSA) developed as part of the Naval Innovative Science and Engineering (NISE)-funded project "Time Domain Switching Proof Mass Proximity Switch Utilization for Inertial Navigation."

The design and fabrication of these devices was based on using a sacrificial layer that both defines a capacitive gap for a sliding, non-contact proximity switch and frees a wafer-thick proof-mass to vibrate in the plane of the wafer.

Time-domain switched accelerometers can be built using a three-mask process. The vacuum-sealing process described in this report is conducted at a low temperature and can be used to vacuum pack the devices on wafer,

15. SUBJECT TERMS

Mission Area: Advanced Integrated Circuit Technology

time-domain switching accelerometer	vacuum switching	shielding noise
three-mask switching	flip-chip bonding	

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
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